INFORMATION PROCESSOR AND CONTROLLER

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Abstract of **JP 10124445 (A)**
PROBLEM TO BE SOLVED: To obtain a device for connecting a storing means with a CPU bus by converting the instruction of access from a CPU to a storing means into a preliminarily decided access command to the storing means which is different from the access command, and supplying the access command. SOLUTION: A CPU 1 is provided with the interface of a CPU bus for specifying a prescribed protocol. A CPU bus has interchangeability with a conventional CPU bus protocol. An address controller 2 has interchangeability with the conventional CPU bus protocol, and the instruction of access from the CPU 1 to a synchronizing memory 3 is converted into a preliminarily decided access command to the synchronizing memory 3 corresponding to this access instruction. Then, an address is instructed through an address bus 5a, and a command being the access command is instructed through a command control bus 5c connected with the synchronizing memory 3. Thus, the synchronizing memory 3 can be directly connected with the CPU bus.